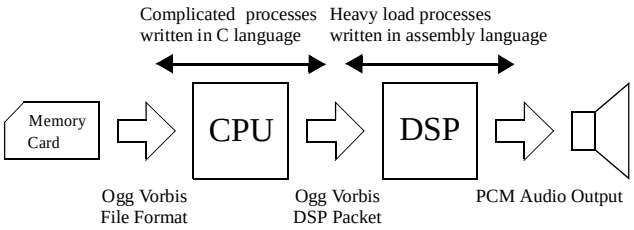
Extremely low power consumption Ogg Vorbis player realized by FineArch One Chip Audio System

Outline

FineArch One Chip Audio System offers an optimal processing environment for a portable music player which demands a small size and a low power consumption. A flexible and high-speed system is built on a single chip by combining a CPU, which can perform complicated processing, a DSP, which has a high throughput, and various kinds of peripherals, necessary for final products. As the first product using this system, we developed the decoding system IP of the Ogg Vorbis; an audio compression format of the next generation known for an open source, a high quality, and high compression ratio. We realized all basic functions needed for a portable audio player, such as file read-out from the memory card, decoding of compression music data, a DAC output, a display of a liquid crystal display, and management of a user interface, on a single chip operating at only 12 MHz system clock. Such a low frequency shows a processing efficiency of our system is more than 6 times higher than that of a system which employs a general CPU only, and lengthens the effective battery life of portable players.

Load Distribution



FineArch One Chip Audio System adopts the multi-core architecture which implements CPU and DSP on a single chip. A management program of the entire system, such as read-out of a file and control of a user interface, are programmed in high level languages, such as C for an easy maintenance, and is processed by the main CPU. On the other hand, a repeating calculation program indispensable to digital signal processings is programmed in an assembly language for giving a higher priority to execution speed, and is processed by the DSP. To develop the Ogg Vorbis decoder system, we tuned up load distribution employing a dual core composition of 1-CPU and 1-DSP, and achieved the remarkably high efficiency. We are now working on the scalable system which implements two or more DSPs with one CPU and will develop a processing system for very high load task such as movie decoders. We plan to support other compression formats such as MP3 and WMA upon request.

Our Original DSP Core

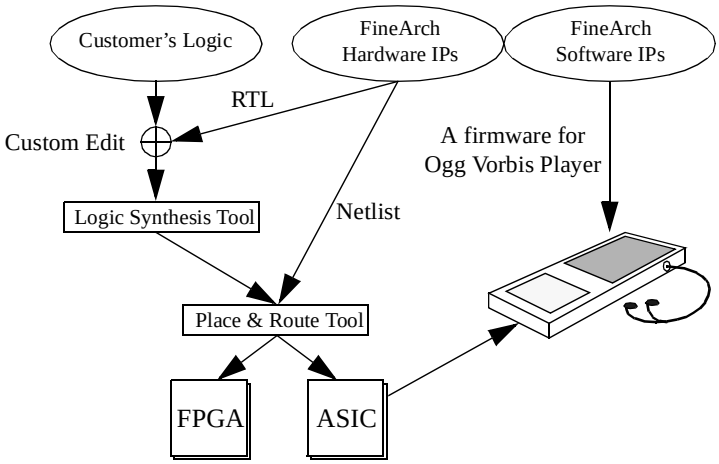
The original DSP core is designed in a manner of 128-bit fixed length VLIW, and can execute simultaneously four commands; an ALU operation, two memory accesses, and a flow control. A powerful addressing mode and transfer mode enables efficient accesses to memory spaces, and a fast processing of repeating calculations dispensable to digital signal processings. From a stage of basic design, the DSP has been designed supposing the multi-core architecture implementation, and has equipped with many features for performing a smooth synchronization with CPU, such as IRQs, interlocks, and a mechanism that allows the CPU to access the internal resorces of the DSP. A step execution function and a break point register are implemented for debugging of DSP programs, and provide a confortable environment to developers.

Key Features

> 128-bit fixed length VLIW
> Simultaneous operation of 4 instructions
> 32-bit fixed point
> Single clock MAC operation
> Size flexible 4 memory spaces
> 16 general purpose data register
> 16 address registers
> Hardware loop counter
> Program counter stack

Hardware and Software IP

Our hardware IPs are designed in fully synthesizable RTL models of VerilogHDL. We can provide our hardware IPs in various formats such as a plane RTL, a netlist, etc., upon customerÅfs request. Customers can use our hardware IP for various uses from an FPGA evaluation to a standard cell ASIC. When the hardware IP is provided in plane RTL, the customer can edit the hardware IP in order to combine with custom logics. Since all software IPs required for an application system are provided with the hardware IPs, product development can be performed easily.

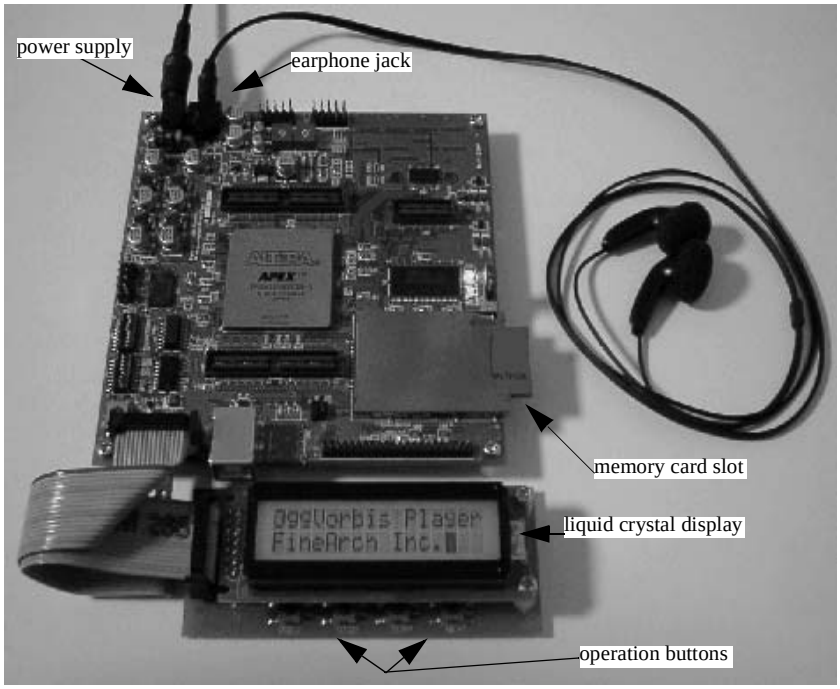


Ogg Vorbis Evaluation Board

We prepared an evaluation board using ALTERA FPGA for developers. We sell it by order-received production. All features necessary for a final product, such as a power supply connector, an earphone jack, a memory card slot, a liquid crystal display, and an operation button, are mounted in this evaluation board.

Specification of the Evaluation Board

>FPGA
ALTERA
>Power
5.0 [V]
>Operating Frequency
12 MHz - 16MHz
>Interfaces
RS232C connector
USB(B-type) connector
ATA drive connection port (44pin)
Logic analyzer extension board connector
SPDIF optical mini jack
Earphone jack
>Memory
1MB SRAM
4MB FLASH
32MB SDRAM
>Supported Memory Card
Memory Stick
SD Card



[About FineArch Inc.]
FineArch is a fabless venture company founded in 2000.
We design system LSI for consumer products.

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[About OggVorbis]
Ogg Vorbis is an open source, and patent and royalty free music compression format. The first official version 1.0 has been released on July, 2002. Especially in lower bit rate (higher compression ratio), Ogg Vorbis has a good reputation of quality of sound compared with that of MP3 and WMA, thus, is very suitable for portable music players demand smaller file size.

Ogg Vorbis Project Home Page
http://www.xiph.org/ogg/vorbis/